

AMENDED CLAIM SET:

1 1. (currently amended) A field effect device, comprising:
2 a crystalline Si body of one conductivity type;
3 a SiGe layer epitaxially disposed on said Si body;
4 a Si layer epitaxially disposed on said SiGe layer; and
5 an insulating layer, on top of which said Si body is disposed thereon; and
6 a source and a drain comprising SiGe in an epitaxial relation with said Si body
7 and connected to each other by said SiGe layer and said Si layer, wherein said source and
8 said drain are formed in recessed source/drain regions of said body, wherein said recessed
9 source/drain regions penetrate all the way down to said insulating layer. said source and
10 said drain having a conductivity type opposite to that of said Si body and each forming a
11 heterojunction and a metallurgical junction with said Si body, wherein said heterojunction
12 coincides with said metallurgical junction with a tolerance of less than about 10nm.

1 2. (canceled)

1 3. (canceled)

1 4. (currently amended) The device of claim 3 1, wherein said insulating layer is SiO₂.

1 5. (original) The device of claim 1, wherein said Si body conductivity is n-type, and
2 wherein a hole device current is confined predominantly in said SiGe layer.

1 6. (original) The device of claim 5, wherein said hole device current is directed along one
2 of a <100> or a <110> crystallographic direction.

1 7. (original) The device of claim 1, wherein said Si body conductivity is p-type, and an
2 electron device current is confined predominantly in said Si layer.

1 8. (original) The device of claim 1, wherein said SiGe layer and said SiGe in said source
2 and said drain are compressively strained.

1 9. (original) The device of claim 1, wherein said SiGe layer is between about 5nm and
2 15nm thick.

1 10. (original) The device of claim 1, wherein said SiGe layer has a Ge concentration
2 which substantially equals a Ge concentration in said SiGe in said source and said drain.

1 11. (original) The device of claim 10, wherein said Ge concentration in said SiGe layer is
2 between about 15% and 50%.

1 12. (canceled)

1 13. (original) The device of claim 1, wherein said device has a top surface plane that lies
2 essentially in one of a (100), (110) or (111) crystallographic plane.

1 14. (original) The device of claim 1, wherein said source and said drain further comprise
2 an epitaxial Si cap layer disposed on top of said strained SiGe, wherein said Si cap layer
3 is between about 2nm and 30nm thick.

1 15. - 17. (canceled)

1 18. (original) The device of claim 1, wherein said Si body conductivity is n-type, and said
2 device is connected in a complementary circuit configuration with an NMOS device.

1 19. (currently amended) A PMOS field effect device, comprising:
2 a crystalline Si body ~~of n-type conductivity~~;
3 a SiGe layer epitaxially disposed on said ~~n-type~~ Si body;
4 a Si layer epitaxially disposed on said SiGe layer; ~~and~~
5 an insulating layer, on top of which said Si body is disposed thereon; and
6 a source and a drain of p-type conductivity comprising SiGe in an epitaxial
7 relation with said ~~n-type~~ Si body and connected to each other by said SiGe layer and said

1 Si layer, wherein said p-type source and said p-type drain are formed in recessed
2 source/drain regions of said n-type body, wherein said recessed source/drain regions
3 penetrate all the way down to said insulating layer, said source and said drain each
4 forming a heterojunction and a metallurgical junction with said n-type Si body, wherein
5 said heterojunction coincides with said metallurgical junction with a tolerance of less than
6 about 10nm.

1 20. (canceled)

1 21. (canceled)

1 22. (currently amended) The device of claim 2+ 19, wherein said insulating layer is SiO₂.

1 23. (original) The device of claim 19, wherein said SiGe layer is between about 5nm and
2 15nm thick.

1 24. (original) The device of claim 19, wherein said SiGe layer has a Ge concentration of
2 between about 15% and 50%.

1 25. (original) The device of claim 24, wherein said Ge concentration in SiGe layer
2 substantially equals a Ge concentration in said SiGe in said source and said drain.

1 26. - 37. (canceled)

1 38. (currently amended) A processor, comprising:

2 at least one chip, wherein said chip comprises at least one field effect device, and
3 wherein said at least one field effect device comprise:

4 a crystalline Si body of one conductivity type;

5 a SiGe layer epitaxially disposed on said Si body;

6 a Si layer epitaxially disposed on said SiGe layer; and

7 an insulating layer, on top of which said Si body is disposed thereon; and

8 a source and a drain comprising SiGe in an epitaxial relation with said Si body

9 and connected to each other by said SiGe layer and said Si layer, wherein said source and

10 said drain are formed in recessed source/drain regions of said body, wherein said recessed

11 source/drain regions penetrate all the way down to said insulating layer. said source and

12 said drain having a conductivity type opposite to that of said Si body and each forming a

13 heterojunction and a metallurgical junction with said Si body, wherein said heterojunction

14 coincides with said metallurgical junction with a tolerance of less than about 10nm.

1 39. (canceled)